Enhancement mode PHEMT Low Noise Amplifier with LNA Linearity Control (IP3) and Mitigated Bypass Switch

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Abstract — **A new LNA has been designed using single supply enhancement mode PHEMT process for WCDMA and other wireless application up to 6GHz. The LNA has direct CMOS logic controllable integrated bypass-mitigated switch and LNA linearity (IP3) control switch. Two different kind of logic controls (0/3V, 3/0V) switch has been design for bypass-mitigated switch. In high linearity mode the LNA draws 8.5mA current and has 15dB gain, 1dB noise figure, -6dBm $IP_{1dB,}$, 7.3 dBm IIP3 with I/O return loss >11dB. In Low linearity mode the LNA draws 3.5mA current and has 14dB gain, 1.1dB noise figure, , -6.5dBm $IP_{1dB,}$, 2dBm IIP3 with I/O return loss >11dB. The LNA bypass-mitigated switch has <3.5dB insertion loss & NF, I/O return loss >11dB and draws negligible current with 3/0V logic, ~200μA for 0/3V logic. Due to well-behaved match of LNA in High Linearity/Low Linearity/Bypass modes, this LNA has minimum mismatch effect for duplexers and filters in a receiver system.**

I. INTRODUCTION

Modern handset and other wireless front end design require a smart switchable current efficient LNA, which can switch it modes easily using a digital controlled logic, depending on incoming signal strength and thus can save battery life and signal integrity without affecting total receiver system performance.

A receiver typically operates in three-signal zone. First, when it is close to a base station, the signal strength is very high and receiver sensitivity is not an issue but distortion or the saturation is the problem. In this situation, LNA is bypassed (**BP**) and mitigated-bypass switch is turned on, it helps to save current and increases the system linearity and power handling capability. When the receiver is at far end zone from base station, LNA works in high linearity (**HL**), high gain mode, because of weak incoming signal and high Tx-Rx leakage, this LNA mode consumes maximum current and provides max. LNA gain, P_{1dB} and IIP3. There is a third in between zone, where the signal strength is medium and it does not require LNA in high linearity mode but needs moderate LNA gain, P_{1dB} and IIP3, in this zone. The LNA is turned on in the low linearity (**LL**), mode and operates at less than half current and provides a little lower performance than high linearity mode.

Previous reported [1-4] LNA/Bypass switch was designed using depletion mode PHEMT process and had high insertion loss and external current setting element. This design uses a (single positive supply) enhancement mode PHEMT process and has a very simple broadband bypass-mitigated switch and a new feature of linearity (IP3) change switch. Also this design has better RF performance in terms of insertion loss, NF and I/O match. Switch design using a enhancement mode PHEMT process is a little challenging compared to a depletion mode PHEMT. For WCDMA and most of the other conventional wireless receiver application, the LNA-Switch operates between the duplexer and an image reject filter. It is therefore important that LNA-Switch should provide a decent match to these elements in all the modes (HL, LL, and BP), otherwise there may be a significant gain ripple in the signal pass band or filter response shift which would degrade system performance. To minimize these effects a mitigating circuit has been included in LNA-bypass Switch path. This circuit helps the switch path to maintain I/O impedance close to LNA's I/O impedance and thus avoids any mismatch between two states and a simple external L, C match can be used for a decent match at any frequency of interest for all LNA modes.

II. CIRCUIT DESIGN

The schematics of LNA designed are shown in fig.1(a), (b) for two different digitally controllable switch to enable/disable LNA/Switch. Each circuit is using three main (0.5μm x 200μm) FETs. FET3 is an amplifier FET and devices X3 and X5 are Switching FEts. Small series source degeneration has been used in amplifying FET (FET3) to improve the NF, I/O match and stability. Very small amount of shunt feedback has also been used in the amplifying FET (FET3) to improve the stability and also to help the I/O match. The amplifier and bypass switch circuit of fig.1(a) and fig.1(b) are similar but their digital controllable switch circuit are different and opposite to each other. Brief description of circuit shown in fig. 1(b) is given here. The port num. 1 & 2 are RF I/O of the circuit and port 2 is also providing bias to LNA drain, and gate

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through a current mirror FET6. Port 3 (LC) is LNA's linearity control switch and need digital ON/OFF (3/0V) logic to turn the LNA linearity in high or low. Port 4 (BP) is the main digitally controllable switch which enables and disables the LNA/Switch when 3/0V is applied to it. When BP=3V, FET5 (fig.1b) is turned on and it activates the current mirror FET6, which helps to bias the gate of FET3, In the bypass path it also turns on device X6, which brings the gate of device X3 and X5 to 0V. Since this is a enhancement mode process, 0V turns the devices X3 and X5 off, so Bypass path is disabled. When BP=3V and LC=0V, LNA works in Low linearity mode, because R2 and R3 set the current of current mirror. When BP=3V and LC=3V, LNA works in High Linearity mode, because FET4 is on and this shorts R3, so only R2 sets the current of current mirror. If, BP=0V, this turns off the FET5 and so current mirror FET6 and LNA FET are is disabled. Drain Voltage of the LNA/Switch provides gate voltages at Devices X3, X5 and X7through R5. This gate Voltage turns the X3, X5 and X7 ON. So, this condition enables the Bypass mode and disables the LNA mode. X7 helps to bring R9 to 0V and this makes Vg of FET3 hard ground. PRC acts as an mitigator for bypass mode, which helps to nearly duplicate LNA I/O impedance in Bypass path and thus minimize the mismatch between LNA and bypass modes.

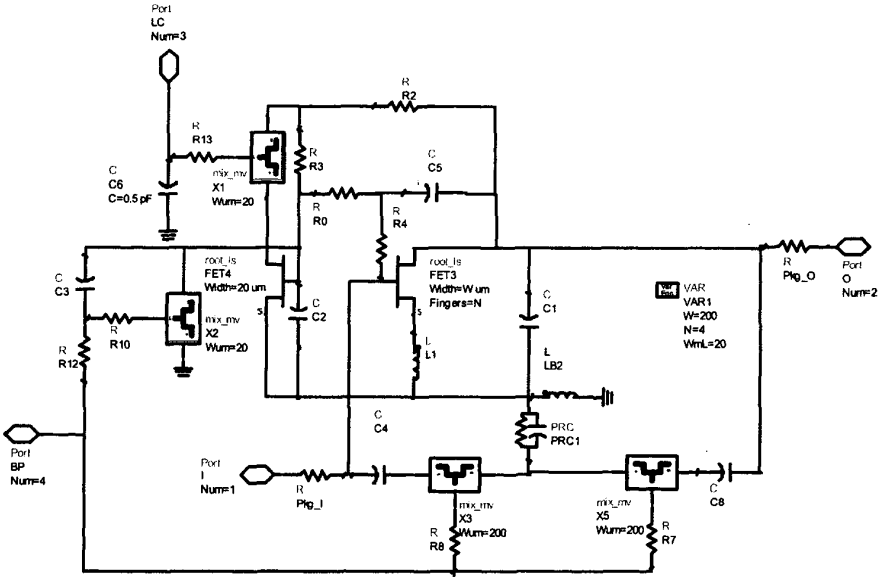
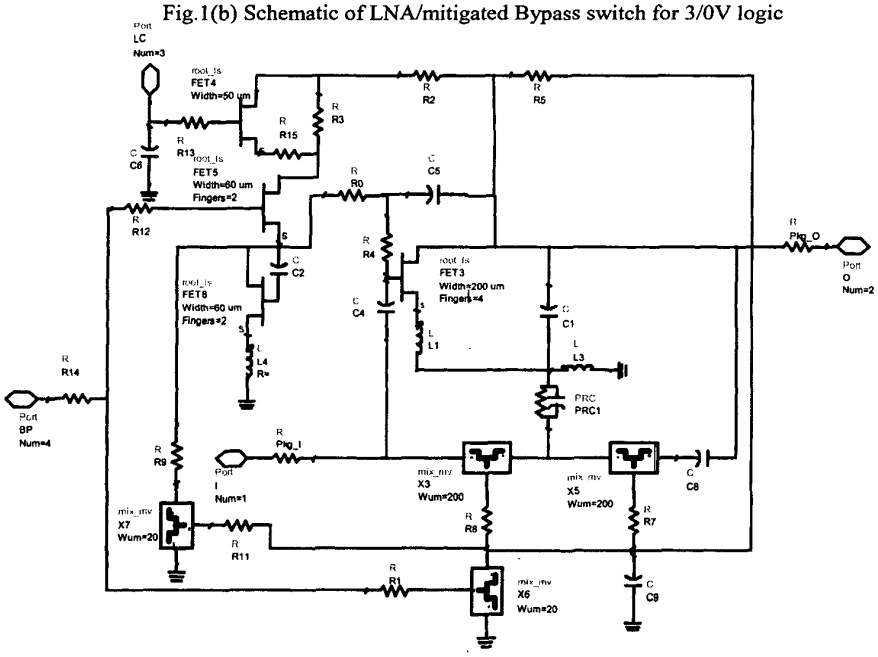


Fig.1(a) Schematic of LNA/mitigated Bypass switch for 0/3V logic

Fig.1(b) Schematic of LNA/mitigated Bypass switch for 3/0V logic



Root model has been used for all the active FETs and a large siganl model has been developed for switching FET. The switching FET model has been implemented in ADS using equation based nonlinear SDD.

III. MEASURED PERFORMANCE

A simple L, C elements have been used to match device I/Os with 50 ohm ports. Some of the measured performance is tabulated in table 1 and rest are shown in fig.2(a-c).

	@ 2.14GHz	@ 5.3 GHz
S21 (HL)	See the graph	11.4 dB
S21 (LL)	See the graph	10.3 dB
S21 (BP)	See the graph	-4.7 dB
S11 (HL)	-11.5dB	-14.1dB
S11 (LL)	-11.0dB	-13.5 dB
S11 (BP)	-11.5dB	-14.0 dB
S22 (HL)	-14.5 dB	-19.6 dB
S22 (LL)	-12.0 dB	-26.1 dB
S22 (BP)	-11.3 dB	-9.0 dB
IIP3 (H.L.)	7.3 dBm	-
IIP3 (L.L.)	2.7 dBm	-
IIP3 (B.P.)	15 dBm	-

Table 1 : Measured performance of LNA @2.14GHz & 5.3GHz

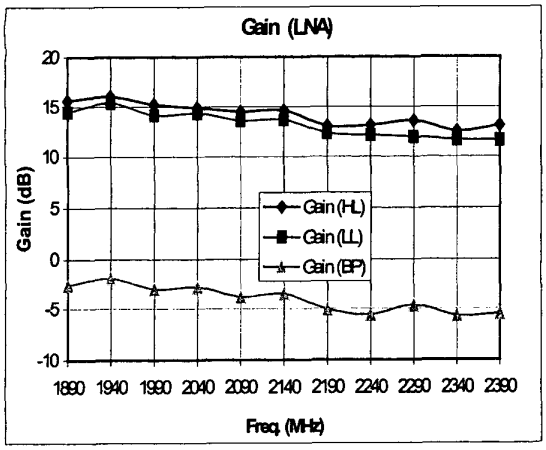


Fig.2(a)

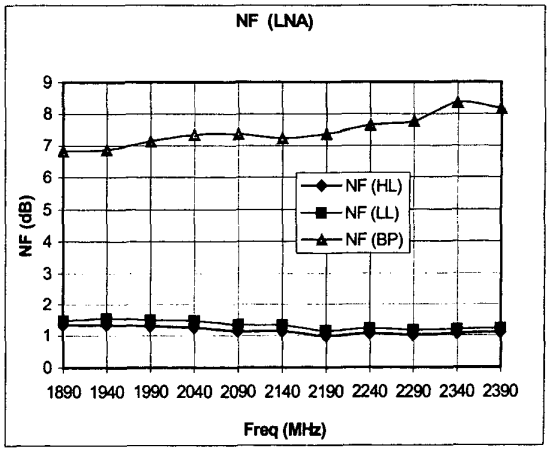


Fig.2(b)

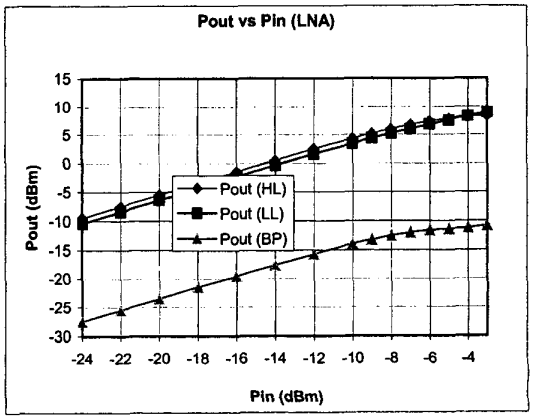


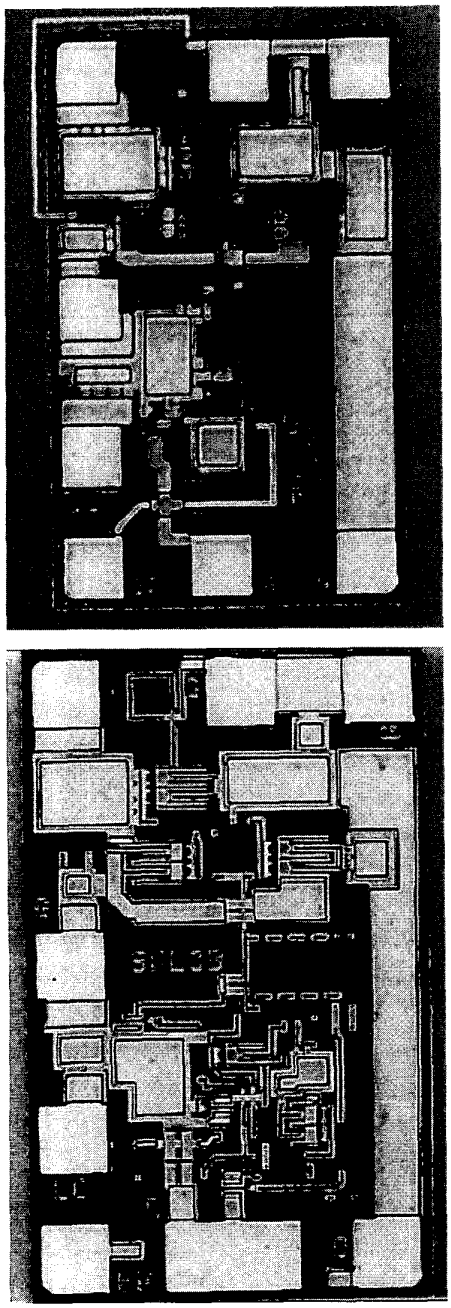
Fig.2(c)

Fig.2 a,b,c, measured performance of LNA

IV. SUMMARY

A new high performance enhancement mode LNA has been designed. This LNA has digitally controllable LNA linearity (IP3) and mitigated LNA Bypass switches. The LNA is well matched in all the operational mode and

thus minimizes the impedance mismatch in the receiver chain.



Photograph of LNA/Mitigated Bypass Switch with 0/3V logic & 3/0V logic
Chip Size : 500um x 740 um

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